INFUSION

Innovations from the NASA CICT Program

CICT

Computing, Information, and Communications Technology Program

www.cict.nasa.gov

Nanotubes May Break Through "Chip Wall"

- **Carbon nanotube (CNT) research paves way for smaller, faster computers, networks, and sensors**
- **CNT interconnects for silicon chips conduct higher currents and enable more layers**

In 1965, just four years after the first planar integrated circuit (IC) was discovered, Gordon Moore observed that the number of transistors per integrated circuit had grown exponentially. He predicted that this would continue, and the media soon began to call his prophesy "Moore's Law."

For nearly forty years, Moore's Law has been validated by the technological progress achieved in the semiconductor industry. Now, however, industry experts are warning of a "Red Brick Wall" that may soon block the continued scaling predicted by Moore's Law. The "red bricks" in the wall are those areas of technical challenge for which no known manufacturable solution exists. One such "brick" is the challenge of finding a new material and processing technology to replace the metals used today to interconnect transistors on a chip.

NASA is also keenly interested in future chip development because of the need to develop smaller and more complex computer systems for future space missions. CICT's Information Technology Strategic Research (ITSR) Project is investigating new materials and fabrication techniques that could break through the "Red Brick Wall."

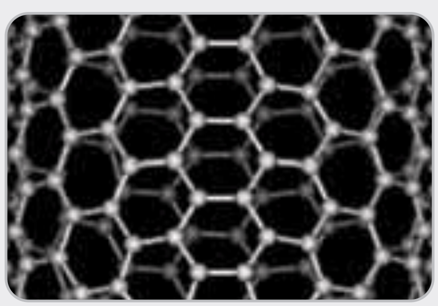
An ITSR team led by Jun Li, senior research scientist at the Center for Nanotechnology at NASA Ames Research Center is exploring ways to integrate ultra-small nanostructured materials into practical devices such as silicon-based ICs.

Harry Partridge, manager of ITSR's bio-nanotechnology research group, says "Jun Li and his colleagues are making great progress combining lithography and other semiconductor processing techniques to build individual nano elements such as carbon nanotubes (CNTs) and semiconducting nanowires (SNWs) into large-scale integrated devices from the bottom up."

IC interconnects from the bottom up

Li and his colleagues recently reported a new bottom-up approach to integrating multiwalled carbon nanotubes (MWNTs) into multilevel interconnects for manufacturing silicon-based ICs. The team's paper, "Bottom-up approach for carbon nanotube interconnects," was published as the cover story in the April 14, 2003 issue of Applied Physics Letters (Vol. 82, No. 15).

continued on next page



At left are carbon nanotubes (CNTs) with silicon (SiO_2) around them. Above is the basic "chicken wire" structure of CNTs.

Technology Spotlight

Technology

Fabrication technique for using carbon nanotubes (CNTs) as interconnects for integrated circuits

Function

Replace copper interconnects on silicon-based integrated circuits

Relevant Missions

- Exploration Systems Enterprise missions
- Aerospace Technology Enterprise missions
- Space Science Enterprise missions
- Biological and Physical Research Enterprise missions
- Earth Science Enterprise missions

Applications

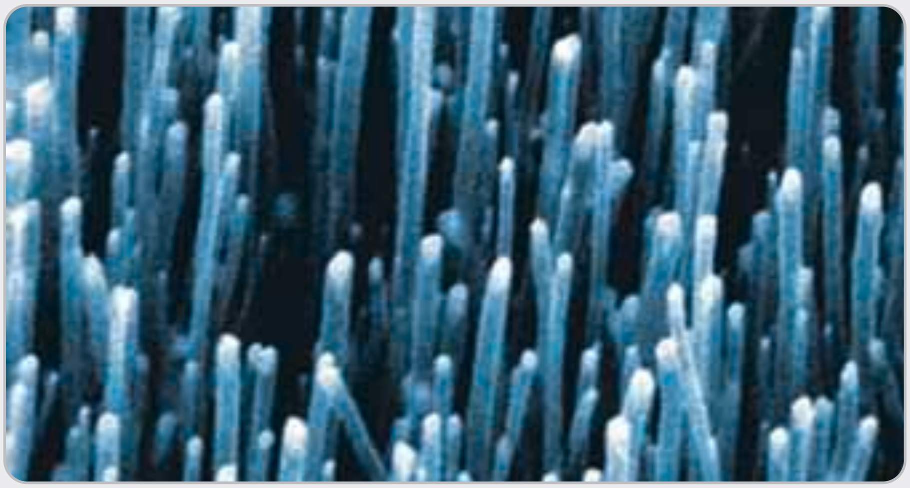
- Micro-devices and sensors for future spacecraft systems
- Computers and networks
- Integrated circuits of all kinds

Benefits

- Enables more electronic layers to be placed on silicon chips
- Enables manufacture of smaller chips
- CNTs conduct higher currents than copper interconnects
- CNTs do not require grooves to be etched in the silicon substrate for placement

Contacts

- jli@mail.arc.nasa.gov
- Harry.Partridge@nasa.gov



These vertically aligned CNTs are about 100 nanometers in diameter and 3 micrometers tall.

In the paper, Li's team demonstrated "a material and processing solution to integrate carbon nanotubes into multileveled interconnects to meet future silicon IC needs. The process sequence—which involves lithography, metallization, plasma deposition of CNTs, dielectric gap-filling, planarization, annealing, etc.—is compatible with current IC manufacturing practice." They also note that, in this new process, "the MWNTs can be grown precisely at desired locations and retain their integrity; thus, they are applicable for multilevel vertical interconnects."

The extraordinary properties of CNTs

Nanotechnology is the creation of functional materials, devices, and systems by controlling matter at the atomic or molecular level—from 1 to 100 nanometers in size. A nanometer is one billionth of a meter—the size of two large atoms. A carbon nanotube can be just a few nanometers in diameter.

First discovered in 1991, the carbon nanotube is a long, thin, cylindrical, hexagonal lattice (graphene) of carbon molecules, one molecule thick, only ten to twenty atoms around, and up to a few thousandths of an inch long. Sometimes called "buckytubes" because they are distended versions of the Buckyball (C60 molecule), CNTs display extraordinary mechanical, electrical, and thermal properties. They can conduct electricity as well as copper, conduct heat as well as a diamond, and are a hundred times stronger than steel at one-sixth of the weight per volume. Their characteristics vary depending on how they are rolled, and how thick they are (single or multi-walled).

High currents with no etching or filling

As copper interconnect lines become thinner than the 130nm used today, their resistance to the flow of electricity increases due to scattering at the surface and grain boundaries, and they tend to break down due to electromigration. This obviously stands in the way of making smaller chips. By contrast, MWNTs show ballistic transportation with little resistance. This unique property and their nanometric scale, opens the door to smaller chip configurations.

"Carbon nanotubes," says Li, "can conduct very high currents, more than a million amperes in a square centimeter area without any deterioration. Today's copper interconnects can't match that."

"Another problem with today's copper conductors," says Li, "is that you have to etch deep, narrow trenches on silicon wafers and the fill them with copper. This presents an increasingly difficult challenge as the feature size keeps shrinking. We reverse the process by building materials one by one from the bottom up, and thus eliminate the etching and filling problems."

As easy as cake

Using the new process discovered by Li and his colleagues, manufacturers will be able to increase computer capability by adding more cake-like layers of components to silicon chips. Li's team used a chemical process to "grow" microscopic, whisker-like CNTs on the surface of a silicon wafer. A layer of silicon dioxide (SiO_2) is then deposited to encapsulate the CNTs and the chip surface (see photo on front page). The top part of the CNTs and part of the SiO_2 are then polished away during planarization.

"With this method," says Li, "manufacturers can build more cake-like layers of electronics on a chip by using vertical carbon nanotube 'wires' to interconnect the layers."

The bottom line

Meyya Meyyappan, director of the Center for Nanotechnology at NASA Ames Research Center and coauthor of the article with Li and others, says, "The bottom line is that computer chips with more layers and smaller components can do more for NASA, which needs high-performance computing in small packages for future autonomous spacecraft. While we are working on carbon nanotube-based chips for NASA's long-term needs, we also are indirectly helping to keep silicon-based computer chips in use as long as possible."

–Larry Laufenberg

For more information or stories online, see **www.cict.nasa.gov/infusion**

NASA CICT Program Office
Ames Research Center
650.604.2494

Program Manager
Butler Hine

Deputy Program Manager
Bill Van Dalsem

Infusion Editor
Larry Laufenberg
llaufenberg@mail.arc.nasa.gov

CICT is part of the NASA Exploration Systems Enterprise's Human and Robotic Technology Theme which represents NASA's commitment to investing in the technologies and capabilities that will make an ambitious and sustainable 21st century space exploration program possible.

www.cict.nasa.gov

CICT